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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/634,736	08/05/2003	Tsuyoshi Yoneyama	9319S-000524	6637

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EXAMINER	
MAI, LAM T	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 06/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/634,736	YONEYAMA, TSUYOSHI	
	Examin r	Art Unit	
	LAM T MAI	2819	

-- The MAILING DATE of this c mmunicati n appears n the cover sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☒ Claim(s) *4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 August 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Drawings

2. Figures 4 and 5 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA (applicant admitted prior art) and further in view of Raatz et al. (USP 5,546,355).

5. Regarding claim 1, AAPA discloses in figure # 4 an integrated circuit that teaches: A serial/parallel conversion circuit (elem. 109) for receiving serial data (DATA) and a clock (CLK) signals, and outputting parallel data; and a memory (elem. 111) for storing the parallel data. AAPA fails to teach a write pulse circuit for

producing/generating a write pulse setting a time for writing data into memory by counting clock signals.

While, Raatz discloses a write pulse generation circuit for using in an integrated circuit memory to allow the integrated circuit memory to operate with clock signals having relatively short duty cycles (please see col. 2, lines 11-14). Raatz also teaches that at high clock frequencies or very short duty cycles, there may not be enough time to successfully write data to a memory cell (please see col. 1, lines 46-49). Therefore, Raatz's write pulse generation circuit is provided to improve this problem.

The applicant describes in specification (page 4, paragraphs 0010 and 0011 and 0012) an identical problem (as taught by Raatz), and an improvement that is integrated a write pulse generation circuit into a convention circuit to improve integrated circuit operation when the cycle of the data writing is shortened.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to employed a write pulse generator circuit taught by Raatz et al. into integrated circuit discloses by AAPA for purpose of improving semiconductor integrated circuit stabilized operation when the cycle of the data writing/reading is shortened.

6. Regarding claim 2, AAPA teaches further in figure # 4, a latch circuit (elem. 110) for latching the parallel data output from the serial/parallel conversion circuit and supplying the data to the memory (elem. 111).

7. Regarding claim 3, AAPA also teaches in figure $ 4, wherein the serial/parallel conversion circuit (elem. 109) includes a shift register.

Allowable Subject Matter

8. Claim 4 is objected to as being dependent upon a rejected base claim, but it would be considered for allowance if it is rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art fails to teach or suggest the write pulse generator circuit that includes following limitations:

a first coincidence detecting circuit detecting coincidence between a count value of the counter and a first predetermined value ;

a second coincidence detecting circuit detecting coincidence between the count value of the counter and a second predetermined value; and

a sequence circuit producing the write pulse by setting an output level to a first level during a period starting from detection of the coincidence by the first coincidence detecting circuit to detection of the coincidence by the second coincidence detecting circuit and by setting the output level to a second level during a period starting from detection of the coincidence by the second coincidence detecting circuit to detection of the coincidence by the first coincidence detecting circuit.

Cited References

8. The prior art made of record and not replied upon is considered pertinent to application's disclosures. The cited references relate write pulse generation circuit applying in integrated circuits and memory circuits.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to LAM T MAI whose telephone number is (571)272-1807. The examiner can normally be reached on 6:00 am - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lam T. Mai
Art Unit 2819